REMARKS

With this Amendment, claims 1, 4, 14-16 are amended; claims 5-13 and 17-19 are cancelled, and new claims 21-32 are added such that claims 1-4, 14-16, and 20-32 are pending. Review and reconsideration of the pending claims is respectfully requested.

Claim Rejections – 35 U.S.C. §102

The Examiner rejects claims 1 and 3 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,689,425 to Sainio et al. Applicants disagree.

Claim 1 has been amended to more particularly define a binary correlator, i.e., as operating on a plurality of pixel data values that are each a single bit. As disclosed in the specification of the present application, the pixel data values are either a logic one or logic zero. Further, claim 1 has been amended to define a binary correlator that is implemented in hardware.

With respect to independent claim 1, Sainio et al. does not disclose or suggest a binary correlator that operates on a plurality of pixel data values that are each a single bit. Further, Sainio does not disclose or suggest a binary correlator that is implemented in hardware, as defined by claim 1.

In particular, the correlator in Sainio operates on a plurality of pixel data values that are 8 bits in size, as the sensor and the analog to digital conversion process provide that level of precision. See column 10, lines 2-13 of Sainio. It would not be obvious to merely replace the 8 bit pixel data values with single bit values, because the selection of an appropriate binary threshold is not easily determined.

Further, the correlator described in Sainio is implemented in software, and operates to compare the relative location of a first color mark to that of a second color mark. In other words, the computer in Sainio is programmed to perform the correlations described therein. See column 13, lines 3-12. The correlations described in Sainio are performed in the frequency domain, and the complexity of the Fourier transforms and inverse Fourier transforms dictate that the correlator be implemented in software.

Therefore, claim 1 defines over the reference cited by the Examiner, and is allowable. Claims 2-4 depend from claim 1, and are allowable for at least the reasons discussed above with respect to claim 1.

Claim Rejections – 35 U.S.C. §103

The Examiner rejects claims 2, 14, 15, and 18-20 under 35 U.S.C. sec. 103(a) as being unpatentable over Sainio et al. in view of U.S. Patent No. 5,917,556 to Katayama. Applicants disagree.

With respect to independent claim 14, claim 14 has been amended to define a correlator that is implemented substantially in hardware. As discussed above with respect to claim 1, Sainio does not disclose or suggest a correlator that is implemented substantially in hardware. Further, Katayama does not cure the deficiencies of Sainio, as Katayama does not disclose a correlator at all. Therefore, claim 14 is allowable. Claims 15-16 depend from claim 14, and are allowable for at least the reasons discussed above.

With respect to independent claim 20, claim 20 requires, inter alia, an image processing subsystem implemented on at least one FPGA, and wherein when it is desirable to change the image processing subsystem, said at least one FPGA is suitably re-programmed. Neither the Sainio, Katayama, nor Zhang references disclose or teach such a re-programmable FPGA, nor does the Examiner point out with particularity how any one of these references teaches this limitation. Accordingly, claim 20 is allowable.

The Examiner rejects claims 4, 5, 7, 8, 9 and 11 under 35 U.S.C. sec. 103(a) as being unpatentable over Sainio et al. in view of U.S. Patent No. 6,295,115 to Zhang et al. Applicants disagree.

With respect to claim 4, claim 4 is dependent upon claim 1, and is allowable for the reasons stated above with respect to claim 1.

New Claims

With respect to new claim 21, claim 21 defines an image processing system adapted to receive and process the image to determine any color register error of the printing press, wherein the image is in the form of a plurality of pixels each having a corresponding data value. The image processing system includes a binarizer for converting data values to corresponding single bit values according to a binarization level. The image processing system also includes a binary correlator using the single bit values and operates to locate register marks on the imprinted paper substrate with respect to the circumferential direction on start up of the press.

Neither the Sainio, Katayama, nor Zhang references disclose or teach either a binarizer or a binary correlator. Further, these references fail to teach a image processing system that operates to locate register marks on the imprinted paper substrate with respect to a circumferential direction of the press on startup of the press. Accordingly, claim 21 is allowable, as are dependent claims 22-28.

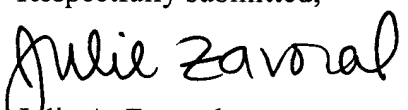
With respect to new claim 29, claim 29 defines an image processing system adapted to receive and process the image to determine any color register error of the printing press. The image is in the form of a plurality of pixels each having a corresponding data value. The image processing system includes a binarizer for converting data values to corresponding single bit values according to a binarization level and a circuit for determining the binarization level according to an analysis of the data values. A binary correlator uses the single bit values and operates to locate register marks on the imprinted paper substrate.

As discussed previously, none of the cited references disclose or teach a binarizer or a binary correlator. Accordingly, claim 29 is allowable, as are dependent claims 30-32.

CONCLUSION

In view of the foregoing, entry of the above amendments and allowance of claims 1-4, 14-16, and 20-32 are respectfully requested. The undersigned is available for telephone consultation at any time.

Respectfully submitted,



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